Applicants respectfully request the following amendments in support of the following remarks.

IN THE CLAIMS:

Please amend the claims as follows.

Claims 1-7 (Canceled)

8. (Currently Amended) A method for identifying false paths, comprising:
providing a path corresponding to a circuit design;
determining whether a set of final value conditions are satisfied;
determining whether a set of side value propagation conditions are satisfied;
determining whether a set of initial value conditions are satisfied;
determining whether one or more slower path conditions are satisfied; and
determining whether the path is false based on ~~at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions~~ whether the set of final value conditions, the set of side value propagation conditions, the set of initial value conditions and the one or more slower path conditions are satisfied.

Claim 9 (Canceled)

10. (Original) The method of claim 8, wherein the set of final value conditions and the set of side value propagation conditions correspond to a first time frame and the set of initial value conditions corresponds to a second time frame, different from the first time frame.

11. (Currently Amended) A method for identifying false paths, comprising:

providing a first set of paths corresponding to the circuit design, the first set of paths having single-path component logic blocks and multiple-path component logic blocks;

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path component logic blocks;

providing a path corresponding to a circuit design by selecting the path from the second set of paths;

determining during a first time frame whether a set of final value conditions are satisfied;

determining during the first time frame whether a set of side value propagation conditions are satisfied;

determining during a second time frame different from the first time frame whether a set of initial value conditions are satisfied; and

determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

12. (Original) The method of claim 8, wherein at least one of determining whether a set of final value conditions are satisfied, determining whether a set of side value propagation conditions are satisfied, and determining whether a set of initial value conditions are satisfied, is performed by an automatic test pattern generation (ATPG) tool.

13. (Currently Amended) A method for false path identification within a circuit design, comprising:

receiving a first set of paths corresponding to the circuit design;

generating timing analysis information associated with the first set of paths;

selecting at least one path of the first set of paths;

providing a set of conditions corresponding to the at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool, ~~the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design,~~ the set of conditions comprising whether a final value condition is satisfied, whether one or more side value propagation conditions are satisfied[~~,~~] and whether an initial value condition is satisfied ~~and whether one or more slower path conditions are satisfied~~;

using the timing analysis information to determine whether one or more slower path conditions are satisfied;

the ATPG tool generating a response to the set of conditions ~~using the ATPG model~~; and

identifying a false path within the first set of paths based on the response from the ATPG tool and the timing analysis information.

14. (Currently Amended) The method of claim 13, further comprising after receiving the first set of paths, translating the first set of paths from a first format to a second format.

15. (Original) The method of claim 13, further comprising:

after receiving the first set of paths, extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths.

16. (Canceled)

17. (Previously Presented) The method of claim 13, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

18. (Currently Amended) A method for false path identification within a circuit design, comprising:

receiving a first set of paths corresponding to the circuit design from a ~~static~~ timing analysis tool;

providing a set of conditions corresponding to at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool, the set of conditions comprising determining whether an initial value condition and a final value condition are satisfied ~~ATPG tool having an ATPG model corresponding to at least a portion of the circuit design~~;

the ATPG tool generating a response to the set of conditions ~~using the ATPG model~~; and

identifying a false path within the first set of paths based on the response from the ATPG tool and whether the one or more slower path conditions are satisfied, wherein a false path report of the false path is fed back to the ~~static~~ timing analysis tool.

19. (Original) The method of claim 13, wherein the ATPG tool is a commercially available ATPG tool.

20. (Currently Amended) The method of claim 13, wherein receiving the first set of paths comprises receiving the first set of paths from a ~~static~~ timing analysis tool.

21. (Currently Amended) A method for identifying false paths comprising:

determining a first set of paths corresponding to a circuit design, the first set of paths having single-path component logic blocks and multiple-path component logic blocks;

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path component logic blocks;

selecting a path from the second set of paths;

determining whether a set of final value conditions are satisfied;

determining whether a set of side value propagation conditions are satisfied;

determining whether a set of initial value conditions are satisfied; and

determining whether the path is false based on ~~at least one of~~ the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

22. (Currently Amended) The method of claim 21, further comprising:

determining whether a set of slower path conditions are satisfied, and

determining whether the path is false ~~is~~ based on ~~at least one of~~ all of the set of final value conditions, the set of side value propagation conditions, ~~and~~ the set of initial value conditions, and the set of slower path conditions.

Claim 23 (Canceled)

24. (Currently Amended) A method for ~~interfacing between a static analysis tool and an automatic test pattern generation (ATPG) tool, capable of~~ identifying false paths within a circuit design with an automatic test pattern generation (ATPG) tool, comprising:

receiving a first set of paths corresponding to the circuit design from a timing analysis tool;

providing a ~~set~~ plurality of sets of conditions corresponding to at least one path of the first set of paths to the ATPG tool, ~~the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design~~ the plurality of sets of conditions comprising a set of final value conditions, a set of side value propagation conditions and a set of initial value conditions;

using the ATPG tool to determine whether the set of final value conditions is satisfied;

using the ATPG tool to determine whether the set of side value propagation conditions is satisfied;

using the ATPG tool to determine whether the set of initial value conditions is satisfied;

using information from the timing analysis tool to determine whether a set of slower path conditions is satisfied;

receiving a response ~~to the set of conditions generated by~~ from the ATPG tool ~~using the ATPG model~~; and

identifying a false path within the first set of paths based on the response from the ATPG tool and the information from the timing analysis tool.

25. (Currently Amended) The method of claim 24, further comprising translating the first set of paths received from the timing analysis tool from a first format to a second format that can be analyzed by the ATPG tool ~~the first set of paths after receiving the first set of paths~~.

26. (Currently Amended) The method of claim 24, further comprising:

extracting a second set of paths from the first set of paths, wherein the ~~set~~ plurality of sets of conditions corresponds to at least one path of the second set of paths.

Claim 27 (Canceled)

28. (Currently Amended) The method of claim ~~27~~ 24, wherein the response to the ~~set~~ plurality of sets of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

29. (Currently Amended) The method of claim 24, further comprising providing a false path report to the ~~static~~ timing analysis tool.

30. (Original) The method of claim 24, wherein the ATPG tool is a commercially available ATPG tool.

31. (Currently Amended) The method of claim 24, wherein timing characterization of circuitry containing the first set of paths is ~~received from the static~~ provided to the timing analysis tool.